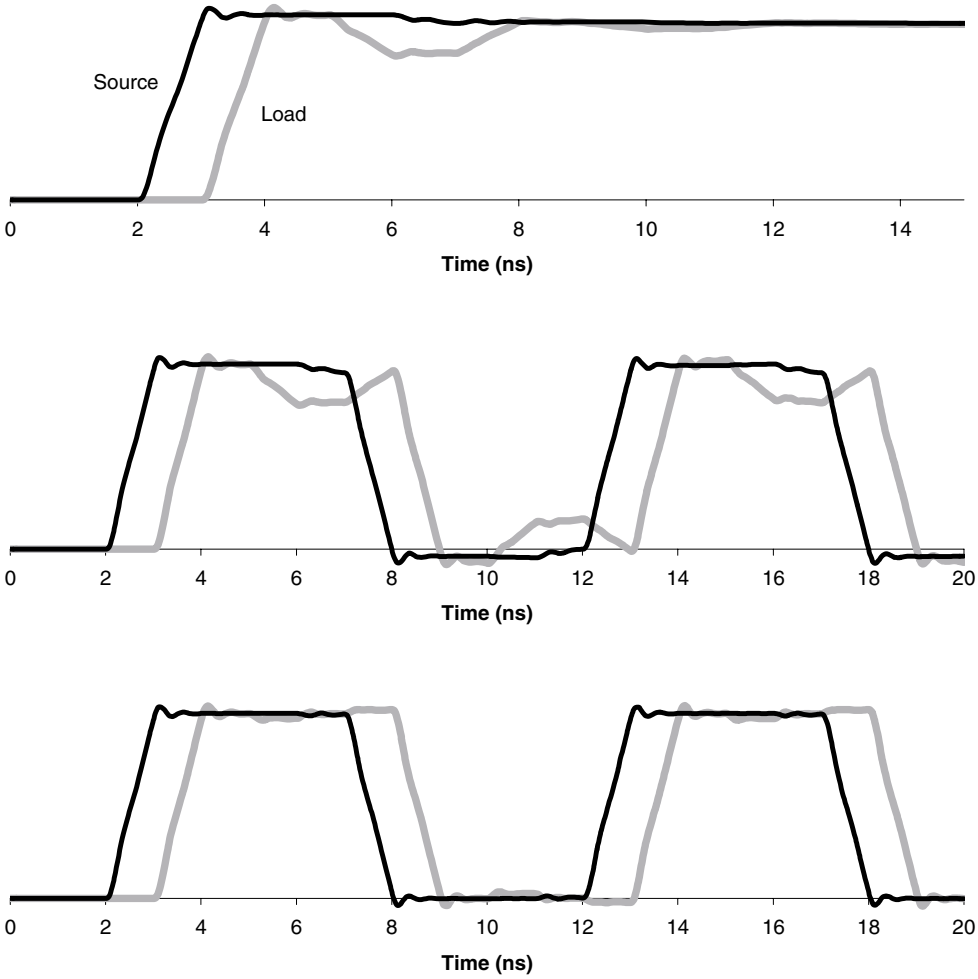

FIGURE 18.2 Transmission line reflections.

$$\text{Microstrip: } Z_O = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left[\frac{5.98H}{0.8W + T}\right]$$

$$\text{Symmetric stripline: } Z_O = \frac{60}{\sqrt{\varepsilon_r}} \ln\left[\frac{1.9(2H + T)}{0.8W + T}\right]$$

$$\text{Asymmetric stripline: } Z_O = \frac{80}{\sqrt{\varepsilon_r}} \ln\left[\frac{1.9(2H_1 + T)}{0.8W + T}\right]\left[1 - \frac{H_1}{4H_2}\right]$$

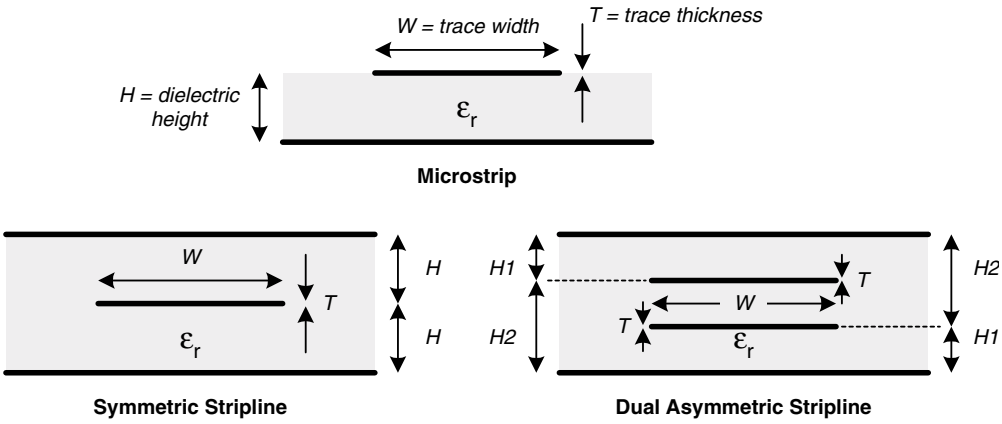

FIGURE 18.3 Microstrip and stripline transmission line topologies.

A type of fiberglass known as FR-4 is a common dielectric found in PCBs. Its relative permittivity is approximately 4.7. Half-ounce copper foil is typically used for signal traces and has an approximate thickness of 0.65 mils. Most PCBs are designed with Z_O between 50 and 75 Ω. These basic constraints lead to typical trace widths of between 4 and 10 mils and typical dielectric heights of 4 mils and higher. Dimensions outside of these ranges are perfectly acceptable and are justified by the requirements of each application. Choosing a trace width is usually based on the packaging technologies and component densities being used. Higher densities usually require finer traces to wire the circuits.

Actual PCB geometries are selected in concert with PCB vendors based on available materials and dimensional requirements. Many circuit boards must conform to a standard thickness so that they can plug into a system such as a PC. A common PCB thickness is 62 mils, roughly 1/16th of an inch. Figure 18.4 shows a sample stack-up using FR-4 and 0.5-oz copper that might be provided by a PCB vendor. This PCB has six layers configured as two power planes and four signal layers with $Z_O = 50$ Ω. Each signal layer uses 8-mil traces. The top and bottom signal layers are microstrips, and the internal signal layers are asymmetric striplines. The PCB vendor does not have much flexibility in assigning the dielectric thickness on the outer layers. Inner layers provide significant flexibility, because the asymmetric heights can be traded-off against each other to achieve the desired imped-

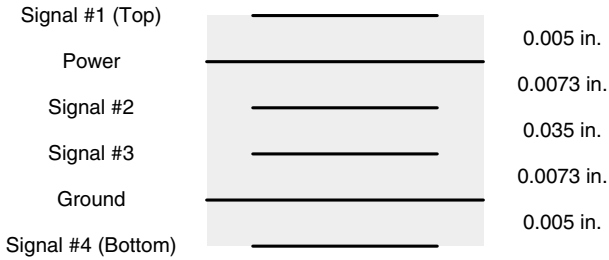

FIGURE 18.4 Sample six-layer PCB stack-up with 0.008-in traces and $Z_O = 50$ Ω.